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(71) Applicant: TDK CORP

(72) Inventor: HAGIWARA ATSUSHI
USUDA MASATO
NAGANO KATSUTO

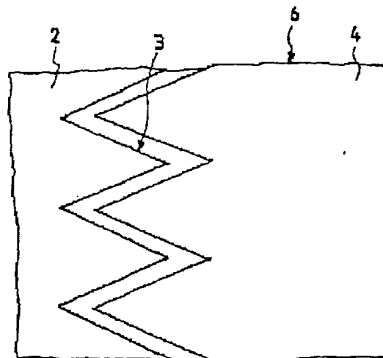
(54) MANUFACTURE OF COLD CATHODE ELECTRON SOURCE surface area.

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(57) Abstract:

PURPOSE: To provide a cold cathode electron source manufacturing method by which cold cathode electron source elements are manufactured stably at low cost in easy processes wherein the elements have a large surface area and show excellent properties.

CONSTITUTION: Manufacture of a cold cathode electron source involves a process to form a resist film on the surface of a conductive layer for an emitter 3 into a wedge-like shape and a process to remove the part of the conductive layer which comes out of the resist film for the emitter 3 by etching, wherein the resist film has smaller surface area of the lower main face in the conductive layer side for the emitter 3 than that of the upper main face, which is a photosensitive face, and has scratches. As a result, cold cathode electron source elements which can exhibit stable and excellent properties by emitters 3 having 50nm or smaller curvature and sharp edge parts are manufactured reproducibly at low cost and high production yield by simple processes and the elements can have a large



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(71) 出願人 000003067

ティーディーケー株式会社

東京都中央区日本橋1丁目13番1号

(72) 発明者 荻原 淳

東京都中央区日本橋1丁目13番1号 ティーディーケー株式会社内

(72) 発明者 薄田 真人

東京都中央区日本橋1丁目13番1号 ティーディーケー株式会社内

(72) 発明者 長野 克人

東京都中央区日本橋1丁目13番1号 ティーディーケー株式会社内

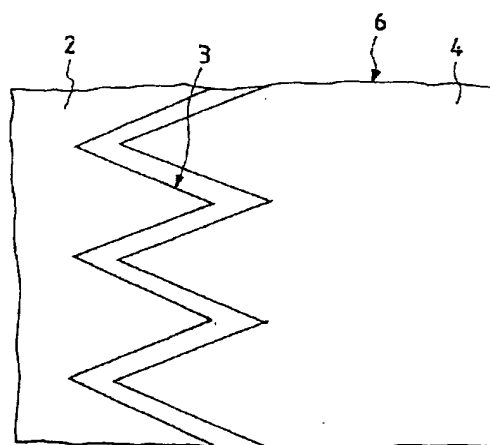
(74) 代理人 弁理士 三澤 正義

(54) 【発明の名称】 冷陰極電子源の製造方法

(57) 【要約】

【目的】 本発明は、簡易なプロセス及び低廉なコストで大面積化が可能で安定かつ良好な特性を発揮し得る冷陰極電子源素子を製造することができる冷陰極電子源の製造方法を提供する。

【構成】 本発明の冷陰極電子源の製造方法は、エミッタ3用導体層表面に、感光面である上主面よりも、前記エミッタ3用導体層側の下主面の面積が小さい庇状を呈するようなレジスト膜を楔状に形成する工程と、前記レジスト膜よりはみ出た前記エミッタ3用導体層をエッチングにより除去する工程を含むものである。これにより、曲率半径50nm以下の尖鋭化された先端をもつエミッタ3による安定かつ良好な特性を発揮し得る冷陰極電子源素子を簡易なプロセスで再現性良く、また低廉なコストで歩留まり良く製造することができ、大面積化が可能となる。



【特許請求の範囲】

【請求項1】 エミッタ用導体層表面に、感光面である上主面よりも、前記エミッタ用導体層側の下主面の面積が小さい底状を呈するようなレジスト膜を楔状に形成する工程と、前記レジスト膜よりはみ出た前記エミッタ用導体層をエッチングにより除去する工程を含むことを特徴とする冷陰極電子源の製造方法。

【請求項2】 ゲート用導体層を付着した後に、前記底状を呈するレジスト膜及びこのレジスト膜表面の前記ゲート用導体層を除去し、尖鋭化した先端をもつ楔状のエミッタを露出させるとともに、このエミッタに前記底状部分の寸法に相当する微小距離を隔てたゲートを対向配置する工程を含むことを特徴とする請求項1記載の冷陰極電子源の製造方法。

【発明の詳細な説明】

【0001】

【産業上の利用分野】 本発明は、冷陰極電子源素子の製造方法に関する。

【0002】

【従来の技術】 電界放射型電子源は、半導体の微細加工技術を利用してミクロンサイズに製造でき、しかも集積化やバッチ加工が容易であるため、熱電子放射型電子源では不可能であったGHz帯増幅器や大電力・高速スイッチング素子、更には高精細度フラットパネルディスプレイ用電子源への応用が期待されており、国内外において盛んに研究開発がなされている。

【0003】 このような電界放射型電子源の従来例を以下に説明する。

【0004】 図21に示す薄膜電界放射型の電子源は、冷陰極52と対向するゲート電極53とを0.3乃至2μmの間隔をあけて絶縁体基板51上に成膜し、真空中で前記冷陰極52とゲート電極53間に電圧をかけることにより電子放出を起こすものである（特開昭63-274047号）。前記冷陰極52はFIB（FocusIon Beam）技術を用いて形成されており、特に凸状部の先端は尖鋭に形成している。しかし、FIB技術を用いた場合、素子の大面積化が困難でかつ製造コストも高くなってしまう。

【0005】 一方、大面積化、製造コストを考えた場合、フォトリソグラフィ技術を用いたパターンニングが妥当である。しかし、現在のフォトリソグラフィ技術では、電子ビームスポット径が最小のパターンニング径となるため、直径0.5μm程度が限界である。このため冷陰極52の先端を尖鋭に形成するには、更に様々なプロセスを加えなくてはならない。しかし、プロセスが増加するほど、その間の素子損傷、特に冷陰極先端部を損傷する可能性が高まり、素子の歩留まりの低下の原因となっている。またそれら冷陰極尖鋭化プロセスのほとんどは煩雑であり、形状制御が困難である。

【0006】 図22に示す薄膜電界放射型の電子源は、

絶縁体基板61上の絶縁層62の表面に、超音波による壁開、破断の方法で冷陰極63、ゲート電極64を平行に形成したものである（特開平3-49129号）。

【0007】 しかし、この図22に示す薄膜電界放射型の電子源の場合、超音波による破断を伴うものであるため、冷陰極63の形状の均一化を図ることが技術的に困難であるとともに、冷陰極63を形成する薄膜に対するダメージが大きいという問題がある。

【0008】 図23、図24に示す薄膜電界放射型の電子源は、フォトリソ技術を用いて絶縁体基板71上の絶縁層72の上に多数の凸状部を持つ冷陰極73を形成した後に、等方性エッチング技術を利用して凸状部の先端を尖鋭化したものである（特開平3-252025号）。尚、図23中、74は冷陰極73と対向するゲート電極である。しかし、エッチング条件による冷陰極73の形状の制御が困難である。さらに、側壁保護膜の形成等によりアンダーカットが進行しないような場合には適用できない。

【0009】 また、エミッターゲート間のギャップ制御については、エミッタ材の上の被覆材を形成した後、アンダーカットが入るようにエミッタをエッチング等により形成し、このエミッタ及び被覆材の上方からゲートを蒸着等により形成する方法がある（特開平4-28138号）。しかし、エッチング条件によるアンダーカットの制御は困難で、再現性、精度の点で問題がある。さらに、側壁保護膜の形成等によりアンダーカットが進行しないような場合には適用できない。

【0010】

【発明が解決しようとする課題】 上述したように、従来の電界放射型電子源の製造方法の場合、冷陰極とゲート電極との距離を制御することが困難であったり、冷陰極の形状を適切に設定できなかったりして、特性が良好で、かつ、安定した電界放射型電子源を得ることができないという問題があった。

【0011】 そこで、本発明は、簡易なプロセス及び低廉なコストで大面積化が可能で安定かつ良好な特性を発揮し得る冷陰極電子源素子を製造することができる冷陰極電子源の製造方法を提供することを目的とするものである。

【0012】

【課題を解決するための手段】 請求項1記載の冷陰極電子源の製造方法は、エミッタ用導体層表面に、感光面である上主面よりも、前記エミッタ用導体層側の下主面の面積が小さい底状を呈するようなレジスト膜を楔状に形成する工程と、前記レジスト膜よりはみ出た前記エミッタ用導体層をエッチングにより除去する工程を含むものである。

【0013】 請求項2記載の冷陰極電子源の製造方法は、ゲート用導体層を付着した後に、前記底状を呈するレジスト膜及びこのレジスト膜表面の前記ゲート用導体

層を除去し、尖鋭化した先端をもつ楔状のエミッタを露出させるとともに、このエミッタに前記底状部分の寸法に相当する微小距離を隔てたゲートを対向配置する工程を含むものである。

【0014】

【作用】請求項1記載の冷陰極電子源の製造方法によれば、一般に通常行われているフォトリソグラフィを用いて先端の尖鋭化したエミッタを均一にかつ再現性良く形成できるため、低廉かつ大面積化が可能で、ゲート電圧の低電圧化、安定した高い放出電流、高い再現性が得られる。

【0015】請求項2記載の冷陰極電子源の製造方法によれば、適当な露光条件の設定によりエミッタとゲート間の距離を均一にかつ再現性良く近接させることができるため、ゲート電圧の低電圧化、安定した高い放出電流、高い再現性が得られる。

【0016】

【実施例】以下に、本発明の実施例を詳細に説明する。

【0017】（実施例1）図1に示すように絶縁性基板1、例えばガラス基板の表面に、0.3 μ m厚のMoからなる導体層2をスパッタリングにて形成する。次に、図2に示すように前記導体層2の表面に、図2に示すように、スピナーにより、厚さ1乃至3 μ mの厚さにレジスト（ZPP2400：日本ゼオン社製）層5aをコーティングし、90℃、90秒間のプリバークを行う。

【0018】次に、図3に示すように、鋸歯状のパターン8をもつマスク9を用いた露光を行って、更に、アルカリ水溶液を用いてレジスト膜5を現像することによって、感光面である上主面よりも、下主面の面積が小さくなる底状を呈するレジスト膜5を形成する。この時のレジスト膜5の底状部分の形状は、図10、図11乃至図18に示すように露光量によって異なる。

【0019】即ち、レジスト膜5の厚さが2 μ m、プリバークが90℃、90秒、露光をPL501Fにて行い、PEB100℃、60秒、現像を2.38%TMAH65秒パドルで行った場合、露光量1.5で底状部分の寸法は3.4 μ m、露光量2.0で底状部分の寸法は1.8 μ m、露光量2.5で底状部分の寸法は1.0 μ m、露光量3.0で底状部分の寸法は0.9 μ m、露光量3.5で底状部分の寸法は0.8 μ m、露光量4.0で底状部分の寸法は0.7 μ mであった。即ち、底状部分の寸法は露光量によって決定され、これにより、後述するエミッタ3とゲート6との間の距離を調整することができる。

【0020】この後、ポストバークを行う。

【0021】次に、図4、図5に示すように、底状で、かつ、鋸歯状を呈するレジスト膜5よりもはみ出る前記導体層2をドライエッチングにより除去し鋸歯状で尖鋭化した先端をもつエミッタ3を前記レジスト膜5と絶縁性基板1との間に形成する。

【0022】ドライエッチングの条件は、エッチングガスCF₄：O₂=170：30sccm、圧力0.17Torr、RF出力300W、時間10分とする。

【0023】次に、図6、図7に示すように、Ni、Cr、Ta等の金属からなるゲート6用の導体層4を絶縁性基板1に対して垂直方向から入射する条件にて蒸着により成膜する。

【0024】次に、図8、図9に示すように、前記底状で、かつ、鋸歯状を呈するレジスト膜5及びこのレジスト膜5の表面の導体層4を剥離液を用いて除去（リフトオフ）し、尖鋭化した先端をもつ鋸歯状のエミッタ3を露出させるとともに、このエミッタ3に前記底状部分の寸法に相当する微小距離隔てて鋸歯状を呈するゲート6を対向配置する。

【0025】以上の工程により、従来のフォトリソグラフィ技術を利用して、曲率半径50nm以下のエミッタ先端が得られるとともに、冷陰極電子源素子の大面積化が可能となり、しかも製造コストの低廉化をも図れる。

【0026】また、工程数の減少による簡略化が図れ、工程途中の冷陰極電子源の損傷、破壊が低減し歩留まりの向上も図れる。

【0027】更に、自己整合（セルフアライン）プロセスによるゲート6の形成が可能となり、ゲート6-エミッタ3間距離を1 μ m以下に形成可能で、電子放出が容易になり低電圧駆動の冷陰極電子源を得ることができると。

【0028】（実施例2）図19、図20に示すように、絶縁性基板1（ガラス基板）の表面に、保護層10及びSiO₂からなる絶縁層11を形成し、更に、0.3 μ m厚のMoからなる導体層2をスパッタリングにて形成する。

【0029】この後、実施例1と同様な工程で、尖鋭化した先端をもつ鋸歯状のエミッタ3及びこのエミッタ3に前記底状部分の寸法に相当する微小距離隔てて対向する鋸歯状を呈するゲート6を前記絶縁層11の表面に形成する。

【0030】更に、前記絶縁層11にウェットエッチングを施し、エミッタ3、ゲート6の対向領域下部に絶縁層凹部12を形成してエミッタ3、ゲート6を各々前記絶縁層凹部12の空間を隔てて対向させる。これにより、エミッタ3、ゲート6が各々前記絶縁層凹部12の空間を隔てて対向することになり、電子放出効率が向上してより安定かつ良好な特性を発揮し得る冷陰極電子源を低廉なコストで製造することができる。

【0031】

【発明の効果】請求項1記載の発明によれば、曲率半径50nm以下の尖鋭化された先端をもつエミッタによる安定かつ良好な特性を発揮し得る冷陰極電子源素子を簡易なプロセスで再現性良く、また低廉なコストで歩留まり良く製造することができ、大面積化が可能な冷陰極電

子源の製造方法を提供することができる。

【0032】請求項2記載の発明によれば、エミッタに対向したゲートを $1\mu\text{m}$ 以下に近接させて、大面積にわたり均一に配置させることによる安定かつ良好な特性を発揮し得る冷陰極電子源素子を簡易なプロセスで再現性良く、また低廉なコストで歩留まり良く製造することができる冷陰極電子源の製造方法を提供することができる。

【図面の簡単な説明】

【図1】本発明の実施例1における冷陰極電子源の製造工程を示す断面図

【図2】本発明の実施例1における冷陰極電子源の製造工程を示す断面図

【図3】本発明の実施例1における冷陰極電子源の製造工程を示す断面図

【図4】本発明の実施例1における冷陰極電子源の製造工程を示す断面図

【図5】本発明の実施例1における冷陰極電子源の製造工程を示す平面図

【図6】本発明の実施例1における冷陰極電子源の製造工程を示す断面図

【図7】本発明の実施例1における冷陰極電子源の製造工程を示す平面図

【図8】本発明の実施例1により得られる冷陰極電子源の断面図

【図9】本発明の実施例1により得られる冷陰極電子源素子の平面図

【図10】本発明の実施例1における底状部分の露光量と寸法との関係を示すグラフ

【図11】本発明の実施例1における底状部分の露光量

と寸法との関係を示す説明図

【図12】本発明の実施例1におけるエミッタとレジスト膜の形状を示す説明図

【図13】本発明の実施例1における底状部分の露光量と寸法との関係を示す説明図

【図14】本発明の実施例1における底状部分の露光量と寸法との関係を示す説明図

【図15】本発明の実施例1における底状部分の露光量と寸法との関係を示す説明図

【図16】本発明の実施例1におけるエミッタとレジスト膜の形状を示す説明図

【図17】本発明の実施例1における底状部分の露光量と寸法との関係を示す説明図

【図18】本発明の実施例1における底状部分の露光量と寸法との関係を示す説明図

【図19】本発明の実施例2の製造工程を示す断面図

【図20】本発明の実施例2の製造工程を示す断面図

【図21】従来の電子源の一例を示す部分斜視図

【図22】従来の電子源の他例を示す部分斜視図

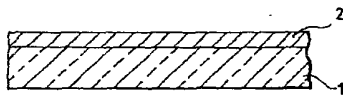
【図23】従来の電子源の更に他例を示す部分斜視図

【図24】従来の電子源の更に他例を示す部分斜視図

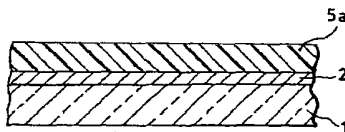
【符号の説明】

- 1 絶縁性基板
- 2 導体層
- 3 エミッタ
- 4 導体層
- 5 レジスト膜
- 6 ゲート
- 11 絶縁層
- 12 絶縁層凹部

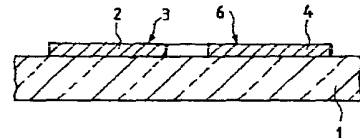
【図1】



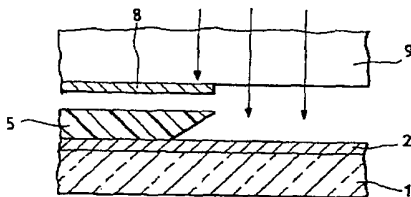
【図2】



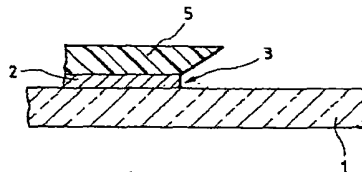
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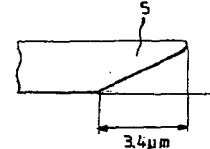
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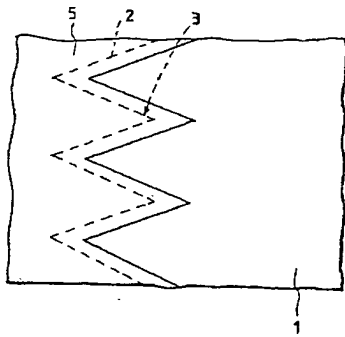
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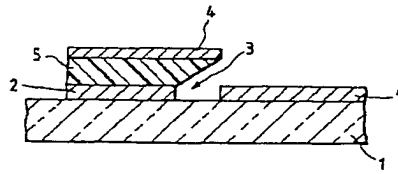
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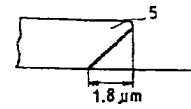
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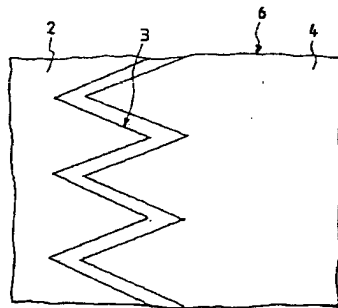
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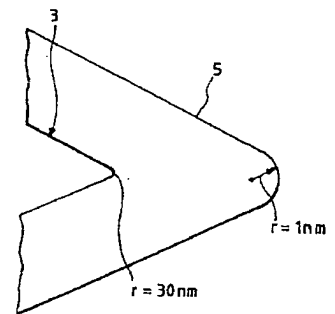
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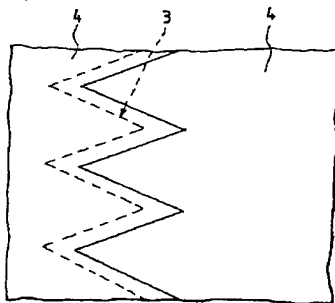
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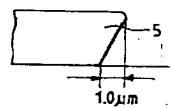
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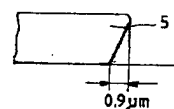
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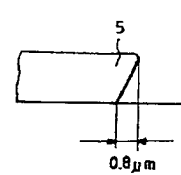
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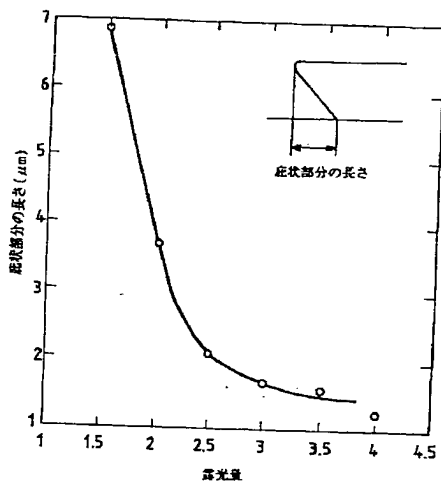
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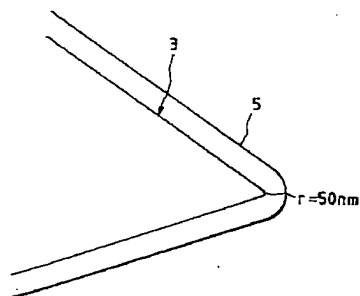
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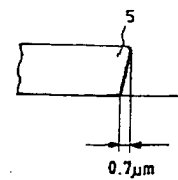
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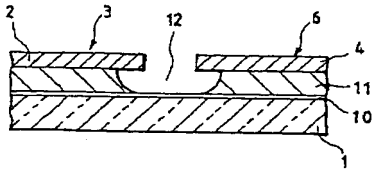
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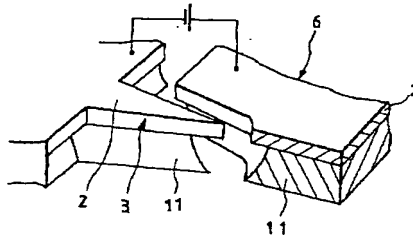
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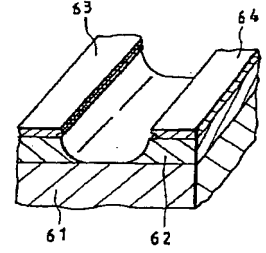
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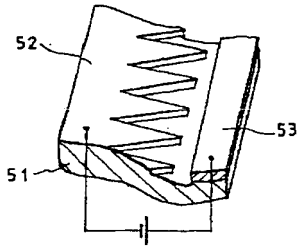
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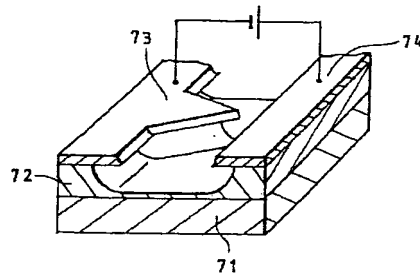
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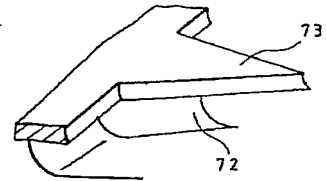
【図21】



【図23】



【図24】



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CLAIMS

[Claim(s)]

[Claim 1] The manufacture method of the cold cathode electron source characterized by including the process which forms in the conductor-layer front face for emitters a resist film which presents the shape of eaves with an area of the lower principal plane by the side of the aforementioned conductor layer for emitters smaller than the upper principal plane which is a sensitization side at a wedge shape, and the process which removes the aforementioned conductor layer for emitters which overflowed from the aforementioned resist film by etching.

[Claim 2] The manufacture method of the cold-cathode electron source according to claim 1 characterized by to include the process which carries out opposite arrangement of the gate which separated the minute distance equivalent to the size of the aforementioned eaves-like portion in this emitter while exposing the wedge-shaped emitter which removes the aforementioned conductor layer for the gates of the resist film which presents the shape of aforementioned eaves, and this resist film front face, and has the radicalized nose of cam, after adhering the conductor layer for the gates.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] this invention relates to the manufacture method of a cold cathode electron-source element.

[0002]

[Description of the Prior Art] A field emission type electron source can be manufactured in micron size using the ultra-fine processing technology of a semiconductor, moreover, since integration and batch processing are easy, by the thermocouple-emission type electron source, the application to impossible GHz band amplifier, and large power and a high-speed switching element, and also the electron source for high definition flat-panel displays is expected, and research and development are briskly made in in and outside the country.

[0003] The conventional example of such a field emission type electron source is explained below.

[0004] The thin film field emission type electron source shown in drawing 21 opens 0.3 or the interval of 2 micrometers, forms cold cathode 52 and the gate electrode 53 which counters on the insulator substrate 51, and causes electron emission by applying voltage between the aforementioned cold cathode 52 and the gate electrode 53 in a vacuum (JP,63-274047,A). The aforementioned cold cathode 52 is formed using FIB (FocusIon Beam) technology, and forms especially the nose of cam of the height acute. However, when FIB technology is used, large-area-izing of an element will be difficult, and a manufacturing cost will also become high.

[0005] On the other hand, when large-area-izing and a manufacturing cost are considered, patterning using photo lithography technology is appropriate. However, with the present Fort Lee SOGUGURA fee technology, since the diameter of the electronic beam spot turns into the minimum diameter of patterning, the diameter of about 0.5 micrometers is a limitation. For this reason, in order to form the nose of cam of cold cathode 52 acute, you have to add still more various processes. However, possibility of damaging the element injury on in the meantime, especially a cold cathode point increases, and it has become the cause of a fall of the yield of an element, so that a process increases. Moreover, most of these cold cathode radicalization processes are complicated, and configuration control is difficult for it.

[0006] The thin film field emission type electron source shown in drawing 22 forms cold cathode 63 and the gate electrode 64 in the front face of the insulating layer 62 on the insulator substrate 61 in parallel by the method of **** by the ultrasonic wave, and fracture (JP,3-49129,A).

[0007] However, since it is a thing accompanied by fracture by the ultrasonic wave in the case of the thin film field emission type electron source shown in this drawing 22, while it is technically difficult to attain equalization of the configuration of cold cathode 63, there is a problem that the damage to the thin film which forms cold cathode 63 is serious.

[0008] The thin film field emission type electron source shown in drawing 23 and drawing 24 is radicalized in the nose of cam of the height using isotropic etching technology, after forming the cold cathode 73 which has much heights on the insulating layer 72 on the insulator substrate 71 using photo etching technology (JP,3-252025,A). In addition, 74 are cold cathode 73 and a gate electrode which counters among drawing 23. However, control of the configuration of the cold cathode 73 by etching conditions is difficult. Furthermore, when an undercut does not advance by formation of a side-attachment-wall protective coat etc., it cannot apply.

[0009] Moreover, about the gap control between the emitter-gates, after forming the covering material on emitter material, there is the method of forming an emitter by etching etc. so that an undercut may enter, and forming the gate by vacuum evaporation etc. from the upper part of this emitter and covering material (JP,4-28138,A). However, control of the undercut by etching conditions is difficult, and has a problem in respect of repeatability and precision. Furthermore, when an undercut does not advance by formation of a side-attachment-wall protective coat etc., it cannot

apply.

[0010]

[Problem(s) to be Solved by the Invention] In the manufacture method of the conventional field emission type electron source, as mentioned above, it could not be difficult to control the distance of cold cathode and a gate electrode, or it could not set up the configuration of cold cathode appropriately, the property was good and there was a problem that the stable field emission type electron source could not be obtained.

[0011] Then, this invention aims at offering the manufacture method of the cold cathode electron source which can manufacture the cold cathode electron-source element which can demonstrate a property possible [large-area-izing], stable, and good at a simple process and cheap cost.

[0012]

[Means for Solving the Problem] The manufacture method of a cold cathode electron source according to claim 1 includes the process which forms in the conductor-layer front face for emitters a resist film which presents the shape of eaves with an area of the lower principal plane by the side of the aforementioned conductor layer for emitters smaller than the upper principal plane which is a sensitization side at a wedge shape, and the process which removes the aforementioned conductor layer for emitters which overflowed from the aforementioned resist film by etching.

[0013] The manufacture method of a cold cathode electron source according to claim 2 includes the process which carries out opposite arrangement of the gate which separated the minute distance equivalent to the size of the aforementioned eaves-like portion in this emitter while exposing the wedge-shaped emitter which removes the aforementioned conductor layer for the gates of the resist film which presents the shape of aforementioned eaves, and this resist film front face, and has the radicalized nose of cam, after adhering the conductor layer for the gates.

[0014]

[Function] Since the emitter with which the nose of cam was radicalized using the photograph process generally performed usually can be formed with uniformly and sufficient repeatability according to the manufacture method of a cold cathode electron source according to claim 1, cheap and large-area-izing are possible, and low-battery-izing of a gate voltage, the stable high emission current, and high repeatability are obtained.

[0015] According to the manufacture method of a cold cathode electron source according to claim 2, since the distance between an emitter and the gate can be made to approach with uniformly and sufficient repeatability by setup of suitable exposure conditions, low-battery-izing of a gate voltage, the stable high emission current, and high repeatability are obtained.

[0016]

[Example] Below, the example of this invention is explained in detail.

[0017] (Example 1) As shown in drawing 1, the conductor layer 2 which consists of Mo of 0.3-micrometer ** is formed in the front face of the insulating substrate 1, for example, a glass substrate, in sputtering. Next, as shown in drawing 2, as shown in drawing 2, by the spinner, thickness 1 or the thickness of 3 micrometers is coated with resist (ZPP2400:Nippon Zeon Co., Ltd. make) layer 5a, and 90 degrees C and prebaking for 90 seconds are performed on the front face of the aforementioned conductor layer 2.

[0018] Next, as shown in drawing 3, the resist film 5 which presents the shape of eaves to which the area of a lower principal plane becomes small is formed rather than the upper principal plane which is a sensitization side by performing exposure using the mask 9 with the serrate pattern 8, and developing the resist film 5 further using alkali solution. The configuration of the eaves-like portion of the resist film 5 at this time changes with light exposure, as shown in drawing 10, drawing 11, or drawing 18.

[0019] 2 micrometers and prebaking Namely, 90 degrees C, 90 seconds, [the thickness of the resist film 5] When it exposed in PL501F and a paddle performs development for TMAH 65 seconds 2.38% for PEB100 degree C and 60 seconds, The size of an eaves-like portion the size of an eaves-like portion with 3.4 micrometers and light exposure 2.0 with light exposure 1.5 1.8 micrometers, light exposure 2.5 -- the size of an eaves-like portion -- the size of an eaves-like portion was [in 1.0 micrometers and light exposure 3.0 / the size of an eaves-like portion of the size of an eaves-like portion] 0.7 micrometers in 0.8 micrometers and light exposure 4.0 at 0.9 micrometers and light exposure 3.5 That is, the size of an eaves-like portion is determined by light exposure and, thereby, can adjust the distance between the emitters 3 and the gates 6 which are mentioned later.

[0020] Then, a postbake is performed.

[0021] Next, as shown in drawing 4 and drawing 5, the emitter 3 with the nose of cam which removed the aforementioned conductor layer 2 which overflows rather than the resist film 5 which is eaves-like and presents serrate by dry etching, and was radicalized in serrate is formed between the aforementioned resist film 5 and the insulating substrate 1.

[0022] The conditions of dry etching are etching gas CF₄: You may be O₂ =170:30sccm, pressure 0.17Torr, RF output 300W, and time 10 minutes.

[0023] Next, as shown in drawing 6 and drawing 7, membranes are formed by vacuum evaporation on the conditions which carry out incidence of the conductor layer 4 for gate 6 which consists of metals, such as nickel, Cr, and Ta, perpendicularly to the insulating substrate 1.

[0024] Next, as shown in drawing 8 and drawing 9, while exposing the serrate emitter 3 which removes the resist film 5 which has the shape of aforementioned eaves and presents serrate, and the conductor layer 4 of the front face of this resist film 5 using exfoliation liquid (lift off), and has the radicalized nose of cam, opposite arrangement of the gate 6 which presents minute distance partition ***** equivalent to the size of the aforementioned eaves-like portion to this emitter 3 is carried out.

[0025] According to the above process, while an emitter nose of cam with a radius of curvature of 50nm or less is obtained using the conventional photolithography technology, large area-ization of a cold cathode electron-source element is attained, and, moreover, cheap-ization of a manufacturing cost can also be attained.

[0026] Moreover, simplification by reduction of the number of processes can be attained, damage on the cold cathode electron source in the middle of a process and destruction decrease, and improvement in the yield can also be aimed at.

[0027] Furthermore, formation of the gate 6 by the self-adjustment (self aryne) process is attained, the distance between the gate 6-emitters 3 can be formed in 1 micrometer or less, electron emission becomes easy, and the cold cathode electron source of a low-battery drive can be obtained.

[0028] (Example 2) it is shown in drawing 19 and drawing 20 -- as -- the front face of the insulating substrate 1 (glass substrate) -- a protective layer 10 and SiO₂ from -- the becoming insulating layer 11 is formed and the conductor layer 2 which consists of Mo of 0.3-micrometer ** is further formed in sputtering

[0029] Then, the gate 6 which presents serrate [equivalent to the size of the aforementioned eaves-like portion / which carries out minute distance partition *****] to the serrate emitter 3 and this serrate emitter 3 which has the radicalized nose of cam at the same process as an example 1 is formed in the front face of the aforementioned insulating layer 11.

[0030] Furthermore, the insulating-layer crevice 12 is formed in an emitter 3 and the opposite field lower part of the gate 6, the space of the aforementioned insulating-layer crevice 12 is separated, and an emitter 3 and the gate 6 are made to give wet etching to the aforementioned insulating layer 11, and to counter respectively. The cold cathode electron source which an emitter 3 and the gate 6 will separate the space of the aforementioned insulating-layer crevice 12 respectively, it will counter, and electron emission efficiency improves by this, and can demonstrate a more stable and good property can be manufactured at cheap cost.

[0031]

[Effect of the Invention] According to invention according to claim 1, the cold cathode electron-source element which can demonstrate the stable and good property by the emitter with the radicalized nose of cam with a radius of curvature of 50nm or less can be manufactured with the sufficient yield with sufficient repeatability at cheap cost by the simple process, and the manufacture method of the cold cathode electron source in which large-area-izing is possible can be offered.

[0032] According to invention according to claim 2, the gate which countered the emitter can be made to be able to approach 1 micrometer or less, and the manufacture method of the cold cathode electron source which can manufacture the cold cathode electron-source element which can demonstrate the stable and good property by making it arrange to homogeneity over a large area with the sufficient yield with sufficient repeatability at cheap cost by the simple process can be offered.

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DESCRIPTION OF DRAWINGS

Brief Description of the Drawings]

- Drawing 1] The cross section showing the manufacturing process of the cold cathode electron source in the example 1 of this invention
- Drawing 2] The cross section showing the manufacturing process of the cold cathode electron source in the example 1 of this invention
- Drawing 3] The cross section showing the manufacturing process of the cold cathode electron source in the example 1 of this invention
- Drawing 4] The cross section showing the manufacturing process of the cold cathode electron source in the example 1 of this invention
- Drawing 5] The plan showing the manufacturing process of the cold cathode electron source in the example 1 of this invention
- Drawing 6] The cross section showing the manufacturing process of the cold cathode electron source in the example 1 of this invention
- Drawing 7] The plan showing the manufacturing process of the cold cathode electron source in the example 1 of this invention
- Drawing 8] The cross section of the cold cathode electron source obtained according to the example 1 of this invention
- Drawing 9] The plan of the cold cathode electron-source element obtained according to the example 1 of this invention
- Drawing 10] The graph which shows the relation of the light exposure of an eaves-like portion and the size in the example 1 of this invention
- Drawing 11] Explanatory drawing showing the relation of the light exposure of an eaves-like portion and the size in the example 1 of this invention
- Drawing 12] Explanatory drawing showing the configuration of the emitter in the example 1 of this invention, and a resist film
- Drawing 13] Explanatory drawing showing the relation of the light exposure of an eaves-like portion and the size in the example 1 of this invention
- Drawing 14] Explanatory drawing showing the relation of the light exposure of an eaves-like portion and the size in the example 1 of this invention
- Drawing 15] Explanatory drawing showing the relation of the light exposure of an eaves-like portion and the size in the example 1 of this invention
- Drawing 16] Explanatory drawing showing the configuration of the emitter in the example 1 of this invention, and a resist film
- Drawing 17] Explanatory drawing showing the relation of the light exposure of an eaves-like portion and the size in the example 1 of this invention
- Drawing 18] Explanatory drawing showing the relation of the light exposure of an eaves-like portion and the size in the example 1 of this invention
- Drawing 19] The cross section showing the manufacturing process of the example 2 of this invention
- Drawing 20] The cross section showing the manufacturing process of the example 2 of this invention
- Drawing 21] The partial perspective diagram showing an example of the conventional electron source
- Drawing 22] The partial perspective diagram showing the other examples of the conventional electron source
- Drawing 23] The partial perspective diagram of the conventional electron source showing other examples further

[Drawing 24] The partial perspective diagram of the conventional electron source showing other examples further

[Description of Notations]

- 1 Insulating Substrate
 - 2 Conductor Layer
 - 3 Emitter
 - 4 Conductor Layer
 - 5 Resist Film
 - 6 Gate
 - 11 Insulating Layer
 - 12 Insulating-Layer Crevice
-

[Translation done.]